REMARKS

Claims 1-18 were pending in this application.

Claims 1 and 12 are amended and claims 19-26 are added. Support for the amendment is found in the specification at p. 3, lines 1-4 and p. 6, lines 8-13. Support for the new claims is found in the original claims. No new matter is added.

Claims 9-11 are withdrawn.

Accordingly, claims 1-8 and 12-26 are now pending in this application.

Applicants request reconsideration of the pending claims in light of the following remarks.

Election/Restriction

Applicants acknowledge the finality of the restriction requirement, and hereby cancel claims 9-11, without prejudice. Applicants reserve the right to file one or more continuation applications for the subject matter of the withdrawn claims.

Claim Rejection under 35 U.S.C. §103

Claims 1, 3-6, 12, and 14-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,196,360 to Doan et al (hereinafter Doan) in combination with U.S. Patent No. 5,766,997 to Takeuchi (hereinafter Takeuchi).

The Office Action urged that Doan in combination with Takeuchi discloses all the elements of claims 1 and 12 of the present invention. (see, Office Action, at page 2 bridging page 3, and page 3 bridging page 4). Applicants respectfully traverse this rejection.

To establish a prima facie case of obviousness, there must be some suggestion, motivation or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in a way that would produce the claimed invention. Applicants respectfully submit that the Patent Office has not made such a showing.

There is no teaching or suggestion in Doan or Takeuchi for a method for fabricating a semiconductor device whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented as in amended claim 1, or the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, lumping of the nickel silicide is prevented,

and a silicide residue is prevented from remaining on the spacers and the field region, as in amended claim 12.

Further, with respect to new claims 19 and 23, there is no teaching or suggestion in Doan or Takeuchi for etching the silicon substrate using an RF sputter etching process to remove particles from the substrate as well as forming a Ni-based metal layer for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed, or on the entire substrate. The Office Action correctly acknowledged that Doan and Takeuchi do not teach the above two steps at page 5 bridging page 6.

Accordingly, applicants respectfully submit that Doan in combination with Takeuchi does not render unpatentable amended claims 1 and 12, and dependent claims 3-6 and 14-17 dependent therefrom respectively, and new claims 19 and 23, and dependent claims 20-22 and 24-26 dependent therefrom respectively.

Applicants respectfully request reconsideration and withdrawal of the rejection to claims 1, 3-6, 12 and 14-17, being unpatentable over Doan and Takeuchi.

Claims 2, 7-8, 13, and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Doan with Takeuchi as applied to claims 1, 3-5, 12, and 14-16 above, and further in view of U.S. Patent No. 6,503,840B2 to Catabay et al (hereinafter Catabay), U.S. Patent No. 6,664,166 B1 to Jaiswal et al (hereinafter Jaiswal) and reasons from the Office Action.

As discussed above, the Office Action correctly acknowledged that Doan and Takeuchi do not teach at what temperature the Ni-based metal layer is formed and using RF sputtering etching to remove particles from the surface of the substrate in-situ with the formation of Ni-based layer and TiN layer. (see, Office Action at page 5 bridging page 6).

With regard to claims 2 and 13, the Office Action further suggests that one of ordinary skill in the art would have been led to the recited temperature through routine experimentation to achieve desired deposition and reaction rates. (see, Office Action at page 6). Applicants respectfully traverse this rejection.

Applicants submit that Catabay and Jaiswal do not provide any disclosure to cure the deficiency in Doan and Takeuchi for a method for fabricating a semiconductor device whereby

the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented as in amended claim 1, or the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region as in amended claim 12.

Further, with regard to new claims 19 and 23, applicants also submit that Catabay and Jaiswal do not provide any disclosure to cure the deficiency in Doan and Takeuchi for forming a Ni-based metal layer for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed, or on the entire substrate. With regard to the Office Action's suggestion that one of ordinary skilled in the art would have been led to the recited temperature through routine experimentation to achieve desired deposition and recitation rates, applicants respectfully disagree. There is no specific disclosure for a Ni-based metal for silicide on a silicon substrate in either Doan or Takeuchi. Although Takeuchi suggests that nickel may replace titanium, Takeuchi nevertheless discloses several metal layers for silicide, including a reaction suppression layer between two metal layers. A person skilled in the art would likely consider that the step for forming a titanium layer for silicide (as in Doan) and a plurality of metal layers (including a reaction preventing layer, as in Takeuchi) on the silicon substrate where the gate pattern and the source/drain region will require a significantly higher temperature than that require for forming a Ni-based metal layer for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed, or on the entire substrate, as in applicants' new claims 19 and 23. This is because titanium has a significantly higher melting temperature than nickel. Catabay and Jaiswal do not cure the deficiency in Doan and Takeuchi with respect to forming a Ni-based metal layer for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed, or on the entire substrate because both Catabay and Jaiswal are silent as to forming a Ni-based metal layer for silicide.

With regard to claims 7-8 and 18, the Office Action urged that Catabay discloses the process wherein the contaminated surface is solvent cleaned to remove residues and then RF cleaned before titanium and then titanium nitride are deposited over the surface of the same chamber (Catabay, abstract). (see, Office Action, at page 5 bridging page 6).

The Office Action further urged that Jaiswal discloses "a method of processing a partially fabricated semiconductor wafer... including performing a wet pre-metallization cleaning step on the surface of the wafer, performing an RF plasma sputter etching process... while maintaining unbroken vacuum conditions ... and depositing a layer of metal on the surface of the wafer ... a stabilization bake cycle then is performed on the wafer", col. 2, lines 50-66. On that basis, the Office Action urged that it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the cleaning and depositing of the combination of Doan and Takeuchi with the teachings of Catabay and Jaiswal because the steps of cleaning/etching and depositing of Catabay and Jaiswal would provide the process of Doan and Takeuchi with continuous process and preventing further contamination. (see, Office Action, at page 6 bridging page 7).

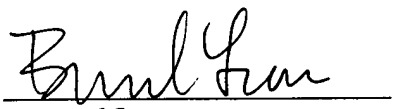
Applicants respectfully submit that the Examiner's piecemeal collection of teachings from several references (4) to arrive at the various elements in the claims, with the benefit of hindsight review of the teachings form the present invention, is improper.

Accordingly, applicants respectfully request reconsideration of the rejections as being unpatentable over the combination of Doan with Takeuchi, and further in view of Catabay and Jaiswal.

For the foregoing reasons, applicants respectfully submit that the instant application is in condition for allowance. Early notice to that end is earnestly solicited.

If a telephone conference would be of assistance in furthering prosecution of the subject application, applicants request that the undersigned be contacted at the number below.

Respectfully submitted,



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